L Number	Hits	Search Text	DB	Time stamp
1	990	("delay chain") and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 07:32
2	227	("delay chain" with inverter) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 07:32
3	38	("delay chain" with inverter with series) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 08:02
4	56	"5621739"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 07:35
5	8	("delay chain" with inverter with even) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 08:11
6	3	("delay chain" with inverter with (tristate tri-state "tri state")) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 08:32
7	1		USPAT	2004/06/23 08:15
8	1		USPAT	2004/06/23 08:20
9	1		USPAT	2004/06/23 08:20
10	1		USPAT	2004/06/23 08:25
11	39	("delay chain" with inverter with clock) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 08:35
12	2	("delay chain" with inverter with known) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 08:38
13	7	("delay chain" with inverter with simple) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 11:17
34	454	(710/240.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 11:18
35	204	(710/241.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 11:23
37	1013	(710/305.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 11:25

38	436	(710/113.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 11:29
39	858	(710/107.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 12:42
40	1252	(710/52.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 12:47
41	354	(326/56.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 12:48
42	344	(327/392.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 12:52
43	334	(713/401.ccls.) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 14:24

44	102	("6141713" "5987549" "4423384" "4897833" "5261109" "5274822" "5649206" "5948078" "6026464" "6301642" "5887267" "4814974" "4969120" "5307466" "4494192" "4924380" "5371893" "5426737" "5699540" "5842025" "5857114" "5884051" "6105094" "4789926" "5513096" "5812880" "6131114" "5918025" "4541043" "4586128" "5682467" "4096572" "4363094" "4536839" "4611297" "4760521" "4768145" "5317696" "5432911" "5506970" "5996037" "6070205" "6240475" "6317813" "6697904" "4928234" "5392434" "5768543" "5598554" "5815681").pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 14:24
-	5014	((tristate tri-state "tri state") adj buffer) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/22 11:08
-	2068	(((tristate tri-state "tri state") adj buffer) same bus) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/22 11:09
-	102	(((tristate tri-state "tri state") adj buffer) same bus same delay) and @ad<20020130	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/23 07:32

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PLUS Search Results for S/N 10060454, Searched June 23, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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10060454_CLS
Most Frequently Occurring Classifications of Patents Returned From A Search of 10060454 on June 23, 2004

Original Classifications

7	710/107
7	710/113
3	710/244
3	711/151
2	710/111
2	710/117
2	710/241

Cross-Reference Classifications

7	710/113
5	710/241
5	711/150
4	710/240
3	710/107
3	710/110
3	711/151
2	340/825.5
2	340/825.51
2	370/462
2	710/108
2	710/119
2	710/242
2	711/168

Combined Classifications

14	710/113
10	710/107
7	710/241
6	711/151
5	710/240
5	711/150
4	710/244
3	710/110
3	710/111
3	710/242
2	340/825.5
2	340/825.51
2	370/462
2	710/108
2	710/112
2	710/116
2	710/117
2	710/119

2 710/22
2 710/309
2 711/158
2 711/168

10060454_CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 10060454 on June 23, 2004

14 710/113 (7 OR, 7 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/113 ..Centralized bus arbitration

10 710/107 (7 OR, 3 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation

7 710/241 (2 OR, 5 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/240 ACCESS ARBITRATING
710/241 .Centralized arbitrating

6 711/151 (3 OR, 3 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/147 .Shared memory area
711/151 ..Prioritized access regulation

5 710/240 (1 OR, 4 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/240 ACCESS ARBITRATING

5 711/150 (0 OR, 5 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/147 .Shared memory area
711/150 ..Simultaneous access regulation

4 710/244 (3 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT

710/240 ACCESS ARBITRATING
710/244 .Access prioritizing

3 710/110 (0 OR, 3 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/110 ..Bus master/slave controlling

3 710/111 (2 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/111 ..Rotational prioritizing (i.e., round robin)

3 710/242 (1 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/240 ACCESS ARBITRATING
710/242 .Decentralized arbitrating

2 340/825.5 (0 OR, 2 XR)
Class 340 : COMMUNICATIONS: ELECTRICAL
340/825 SELECTIVE
340/825.5 .Lockout or priority (programmed or variable)

2 340/825.51 (0 OR, 2 XR)
Class 340 : COMMUNICATIONS: ELECTRICAL
340/825 SELECTIVE
340/825.5 .Lockout or priority (programmed or variable)

340/825.51 ..Designated priority

2 370/462 (0 OR, 2 XR)
Class 370 : MULTIPLEX COMMUNICATIONS
370/431 CHANNEL ASSIGNMENT TECHNIQUES
370/462 .Arbitration for access to a channel

2 710/108 (0 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS

TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/108 ..Bus locking

2 710/112 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/112 ..Bus request queuing

2 710/116 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/113 ..Centralized bus arbitration
710/116 ...Dynamic bus prioritization

2 710/117 (2 OR, 0 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/113 ..Centralized bus arbitration
710/117 ...Time-slotted bus accessing

2 710/119 (0 OR, 2 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation
710/119 ..Decentralized bus arbitration

2 710/22 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/1 INPUT/OUTPUT DATA PROCESSING
710/22 .Direct Memory Accessing (DMA)

2 710/309 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS

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TRANSACTION PROCESSING)

710/305 .Bus interface architecture
710/306 ..Bus bridge
710/309 ...Arbitration

2 711/158 (1 OR, 1 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/154 .Control technique
711/158 ..Prioritizing

2 711/168 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/167 .Access timing
711/168 ..Concurrent accessing

6141713 72
5987549 72
4423384 72
4897833 72
5261109 72
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